7.3inch e-Paper (E)

User Manual

Revision History

Version	Content	Date	Page
1.0	New creation	2024/7/10	All

Contents

1. OVERVIEW

7.3inch e-Paper (E) is a reflective electrophoretic E Ink® Spectra™ 6 technology display module on an active matrix TFT substrate. The panel is capable of displaying black, white, yellow, red, green and blue images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

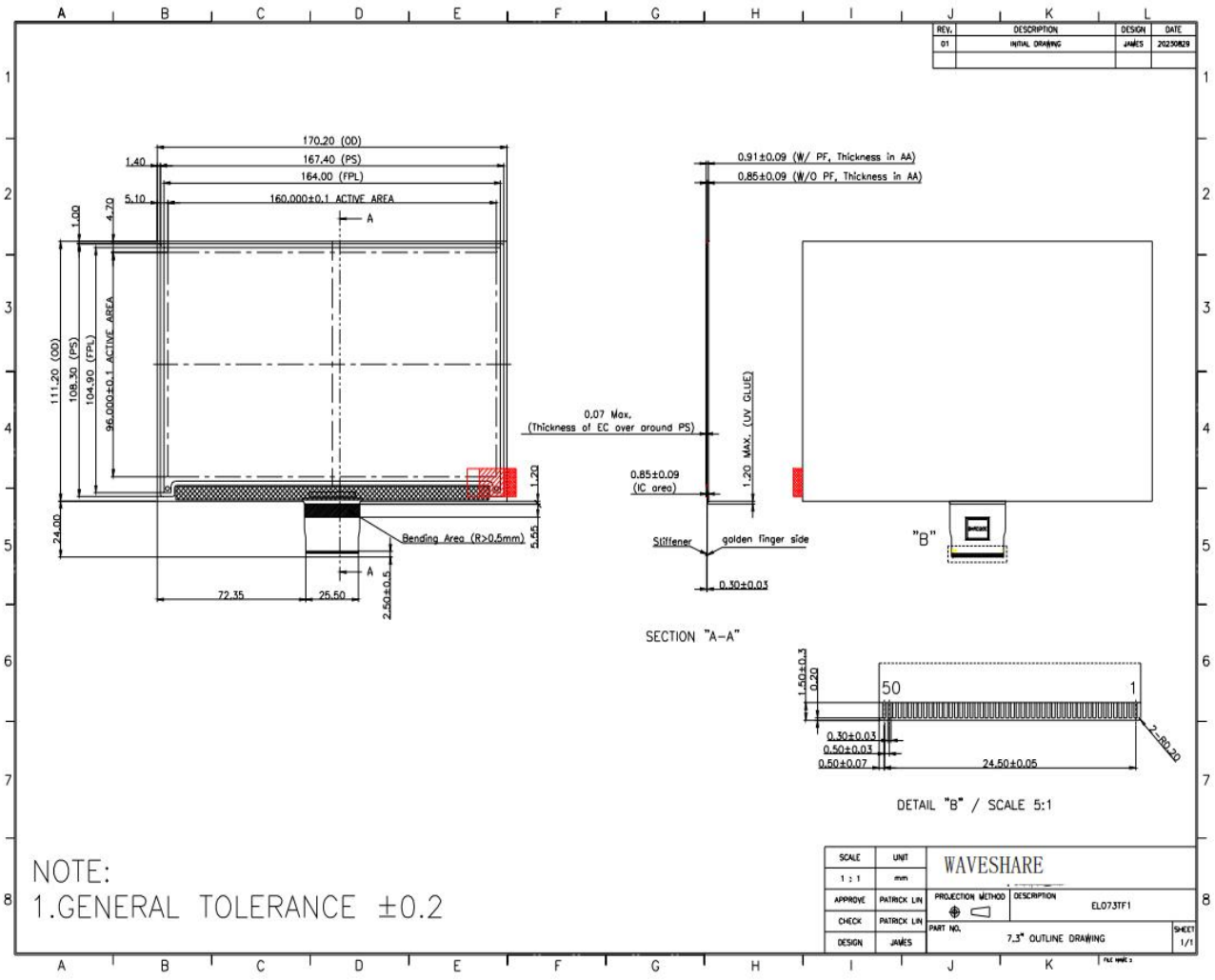
2. FEATURES

- ✧ Highlight Red, Yellow, Green and Blue color
- ✧ High contrast
- ✧ High reflectance
- ✧ Ultra wide viewing angle
- ✧ Ultra low power consumption
- ✧ Pure reflective mode
- ✧ Bi-stable
- ✧ Antiglare hard-coated front-surface
- ✧ Low current deep sleep mode
- ✧ On chip display RAM
- ✧ Waveform stored in On-chip OTP
- ✧ Serial peripheral interface available
- ✧ On-chip oscillator
- ✧ On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- ✧ I2C Signal Master Interface to read external temperature sensor
- ✧ Available in COG package

3. MECHANICAL SPECIFICATION

Parameter	Specification	Unit	Remark
Screen Size	7.3	Inch	
Display Resolution	800 (H) x 480 (V)	Pixel	PPI:127
Active Area	160 (H) x 96 (V)	mm	
Pixel Pitch	0.200 x 0.200	mm	Square
Outline Dimension	170.2 (H) × 111.2 (V) × TBD (D)	mm	Without masking film
Module Weight	TBD	g	

4. MECHANICAL DRAWING OF EPD MODULE



5. INPUT/OUTPUT PIN ASSIGNMENT

5.1 CONNECTOR TYPE: FH34RJ-50S-0.5SH(50)

Pin Assignment (50-pin)

Pin #	Type	Single	Description
1		NC	No connection and do not connect with other NPC pins
2	P	TFT VCOM	TFT_VCOM driving voltage
3	P	FPL VCOM	FPL_VCOM driving voltage
4		NC	NC
5	I/O	GDRH	N-Channel MOSFET Gate Drive Control
6	I/O	RESEH	Current Sense Input for the Control Loop
7		GDRL	Reserved
8	P	GND	Ground
9	I/O	GDRC	P-channel MOSFET Gate Drive Control
10	I/O	RESEC	Current Sense Input for the Control Loop
11	P	VPC	VPC driving voltage
12	P	GND	Ground
13	P	VGL	Negative Gate driving voltage
14	P	VPH	VPH driving voltage
15	P	VSH	Positive Source driving voltage
16	P	VSH LV	Positive Source driving voltage
17	P	VSH LV2	Positive Source driving voltage
18	P	VSL	Negative Source driving voltage
19	P	VSL LV	Negative Source driving voltage
20	P	VSL LV2	Negative Source driving voltage
21	P	GNDA	Ground; Connect to GND
22		REFN	Reserved
23		REEP	Reserved
24	O	TSCL	I2C Interface to digital temperature sensor Clock pin
25	I/O	TSDA	I2C Interface to digital temperature sensor Data pin
26	I	BS0	Bus selection pin; L: 4-wire IF.H: 3-wire IF. (Default)
27	I	BS1	Bus selection pin; L: refer to BS0. (Default) H: Standard 4-wire SPI/dual SPI/quad SPI
28	I	RES#	Reset
29	O	BUSY_N	Busy state output pin
30	I	D/C#	Data/Command control pin (D/C)

Pin #	Type	Single	Description
31	I	CS#	Chip Selection input pin (CSB)
32	I/O	SI0	Serial data pin (SPI)
33	I/O	SI0	Serial data pin (SPI)
34	I/O	SI1	Serial data pin ; Reserved
35	I/O	SI2	Serial data pin ; Reserved
36	I/O	SI3	Serial data pin ; Reserved
37	P	VDDDO	Core logic power pin; Connect to VDDD
38	P	VDD	Supply voltage
39	P	GND	Ground; Connect to GNDA
40	P	VDDIO	Supply voltage
41	P	VCP2	Charge Pump Pin
42	P	CP2N	Charge Pump Pin
43	P	CP2P	Charge Pump Pin
44	P	VCP1	Charge Pump Pin
45	P	CP1N	Charge Pump Pin
46	P	CP1P	Charge Pump Pin
47		CGH1N	Charge Pump Pin; Reserved
48		CGH1P	Charge Pump Pin; Reserved
49	P	VGH	Positive Gate driving voltage
50	P	VCOMBD	VCOMBD driving voltage

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin (BUSY_N) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any command should not be issued to the module. The driver IC would put Busy pin low when the driver IC is working such as:

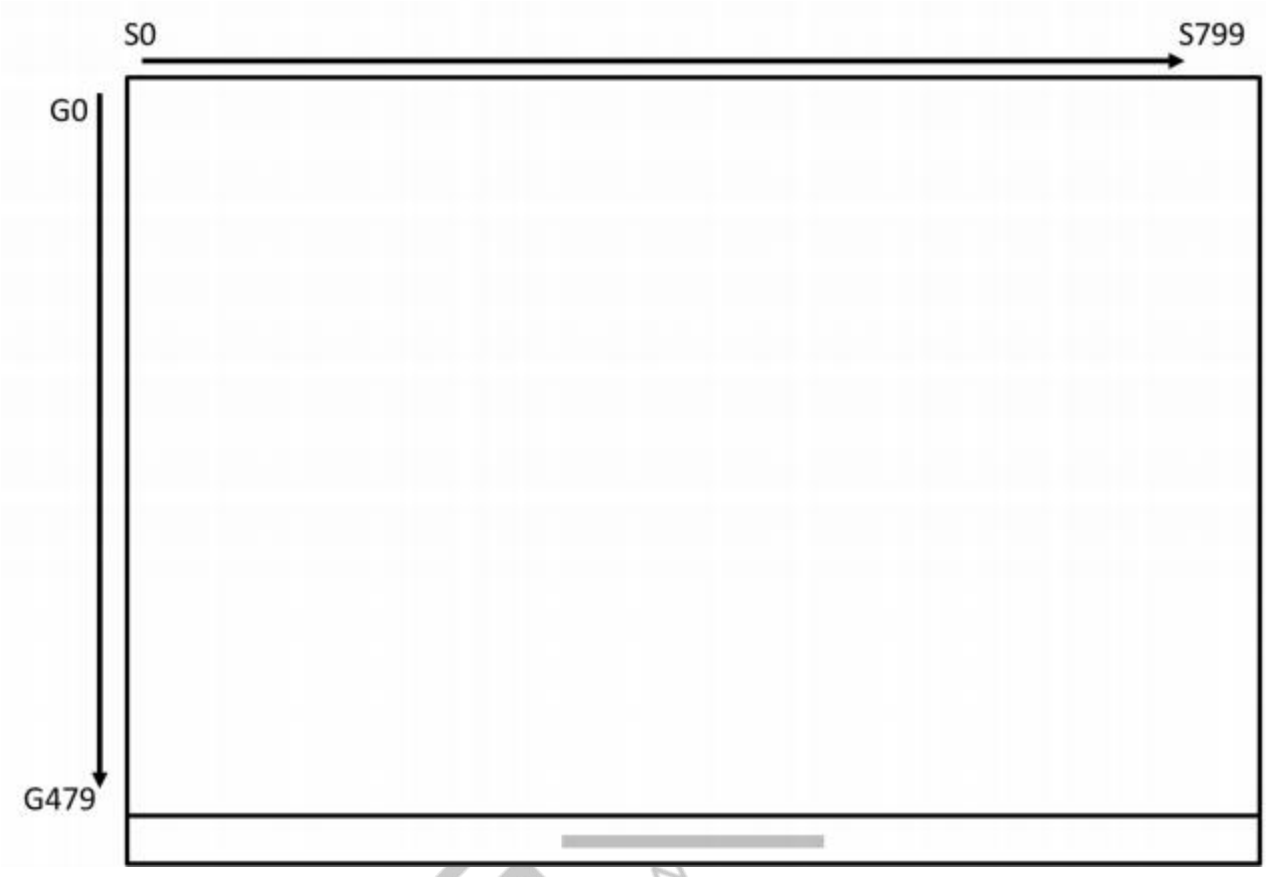
- **Outputting display waveform; or**
- **Programming with OTP**
- **Communicating with digital temperature sensor**

Note 5-5: This pin (BS0) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS0 State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

5.2 PANEL SCAN DIRECTION



6. COMMAND TABLE

W/R: 0: Write cycle; 1: Read cycle; C/D: 0: Command; 1: Data; D7~D0: Don't care

	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Setting
1	Power OFF	0	0	0	0	0	0	0	0	1	0		02h
		0	1	0	0	0	0	0	0	0	0		00h
2	Power ON	0	0	0	0	0	0	0	1	0	0		04h
3	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1		A5h
4	Data Start transmission	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#		--
		0	1	..	..	..	..	..	..	..	..		--
		0	1	#	#	#	#	#	#	#	#		--
5	Data Refresh	0	0	0	0	0	1	0	0	1	0		12h
		0	1	0	0	0	0	0	0	0	1		01h

(1) Power OFF (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power OFF	0	0	0	0	0	0	0	0	1	0
	0	1	0	0	0	0	0	0	0	0

(2) Power ON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power ON	0	0	0	0	0	0	0	1	0	0

(3) Deep Sleep (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver.

(4) Power ON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data Start transmission	0	0	0	0	0	1	0	0	0	0
	0	1	#	#	#	#	#	#	#	#
	0	1	..	..	..	..	..	..	..	..
	0	1	#	#	#	#	#	#	#	#

After this command, data entries will be written into the RAM until another command is written.

(5) Data Refresh (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data Refresh	0	0	0	0	0	1	0	0	1	0
	0	1	0	0	0	0	0	0	0	1

When this command is received. IC will start the refresh process. BUSY_N will become “0”. After the refresh process is finished, BUSY_N will become “1” .

7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS:

Parameter	Symbol	Rating	Unit
Analog power	VDD	-0.5 to +3.6	V
Operating Temp. range	TOPR	(0 to +50)	℃
Storage Temp. range	TSTG	(-25 to +60)	℃

Note:

Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

7.2 DISPLAY MODULE DC CHARACTERISTICS

The following specifications apply for: VDD = 3.0V, VDD 1.8 = 1.8V, TA = 25℃

DIGITAL DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VDD	Logic supply voltage		2.5	3.0	3.6	V
VGH	Positive gate driving voltage		19.0	20.0	21.0	V
VGL	Negative gate driving voltage		-21.0	-20.0	-19.0	V
VSH	Positive source driving voltage		14.5	15.0	15.5	V
VSL	Negative source driving voltage		-15.5	-15.0	-14.5	V
VCOM_DC	VCOM_DC output voltage		-4.0	Adjusted	-0.3	V
VCOM_AC	VCOM_AC output voltage		VSL+ VCOM_DC	VCOM_DC	VSH+ VCOM_DC	V
VIL	Low level input voltage	Digital input pins		-	0.2VDD	V
VIH	High level input voltage	Digital input pins	0.8VDD	-	-	V
VOH	High level output voltage	Digital output pins, IOH = 8mA	0.8VDD	-	-	V
VOL	Low level output voltage	Digital output pins, IOL=8mA	-	-	0.2VDD	V
IMSTB	Module stand-by current	Shut-down				uA
INC	Inrush Current	Booster on	--			mA
IPC	Driving Peak Current	TYP Loading Pattern	--			mA
		High Loading Pattern	--			mA
IMOPR	Module operating current	TYP Loading Pattern	-			mA
		High Loading Pattern	--			mA
P	Operation Power Dissipation	TYP Loading Pattern VDD=3.0V with DC-DC	--			mW
		High Loading Pattern VDD=3.0V with DC-DC	--			mW
PSTBY	Standby Power Dissipation	VDD=3.0V	--		--	uW
IMDS	Module deep sleep current	Deep sleep mode	-		-	uA

Note:

- **The Inrush Current means the inrush current occurs during dual booster on sequence, and it is measured by using Oscilloscope, and extract the Max value**
- **The Driving Peak Current means the peak current occurs during image update after dual booster on sequence, and it is measured by using Oscilloscope, and extract the Max value.**
- **The Module Operating Current data is measured by using Oscilloscope, and extract the Mean value.**
- **The typical loading power consumption is measured using associated 25C waveform with following pattern transition: from full white pattern to color pattern. (Note 7-1)**
- **The high loading power consumption is measured using associated 25C waveform with following pattern transition: from full white pattern to noise pattern (including random scattering of 6 colors) (Note 7-2)**
- **The minimum VDD value by 2.5V is based on typical application pattern with stable and continuing power supply. It does not apply on high loading pattern such as Note 7-2.**
- **The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink**
- **Vcom value has been set in the IC on the panel.**

Note 7-1

The typical power consumption TBD

Note 7-2

The high loading power consumption TBD

7.3 PANEL AC CHARACTERISTICS

7.3.1 MCU INTERFACE

7-3-1-1 MCU INTERFACE SELECTION

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS0 pins. When it is “High”, 4-wire SPI is selected. When it is “Low”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 7-1: MCU interface assignment under different bus interface mode

Note 7-3: Lis connected to GND.

Note 7-4: H is connected to VDD.

7-3-1-2 MCU SERIAL INTERFACE (4-WIRE SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDA, D/C#, CS#.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-5: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

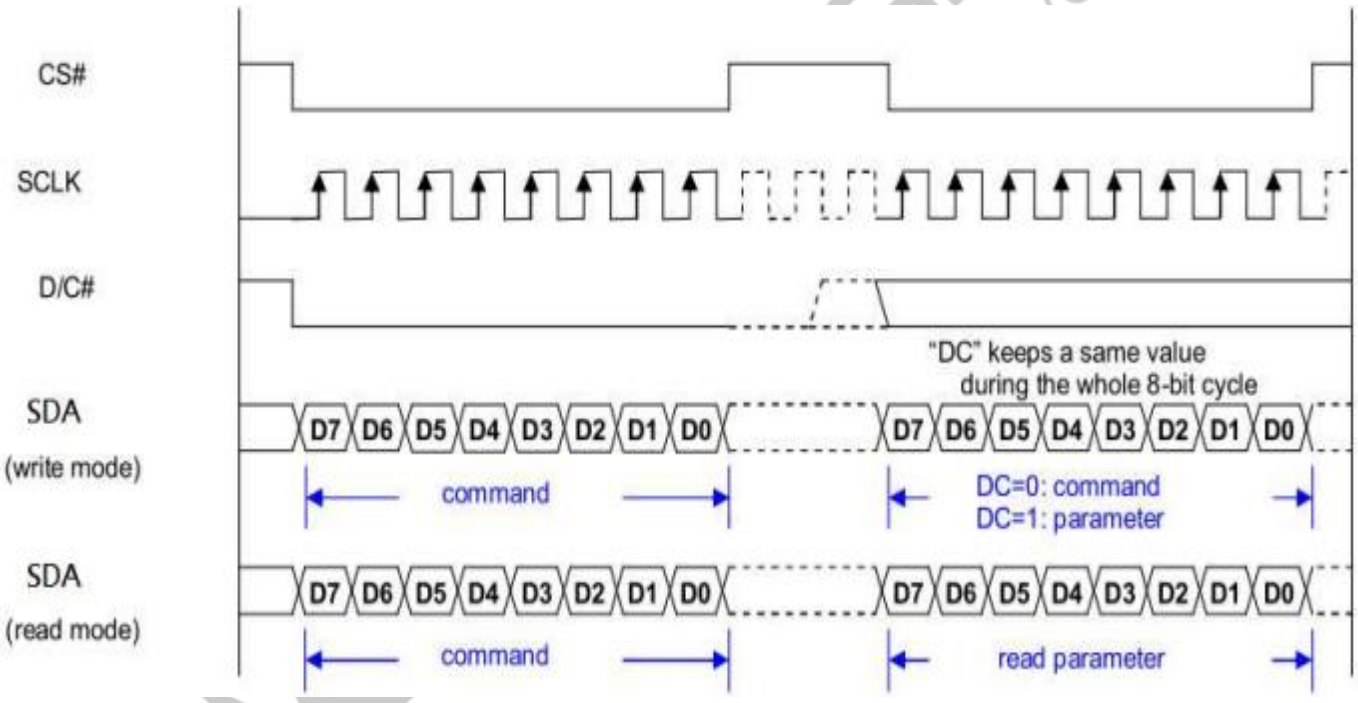


Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode

7-3-1-3 MCU SERIAL INTERFACE (3-WIRE SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDA and CS#. In 3-wire SPI mode, the pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-6: ↑stands for rising edge of signal.

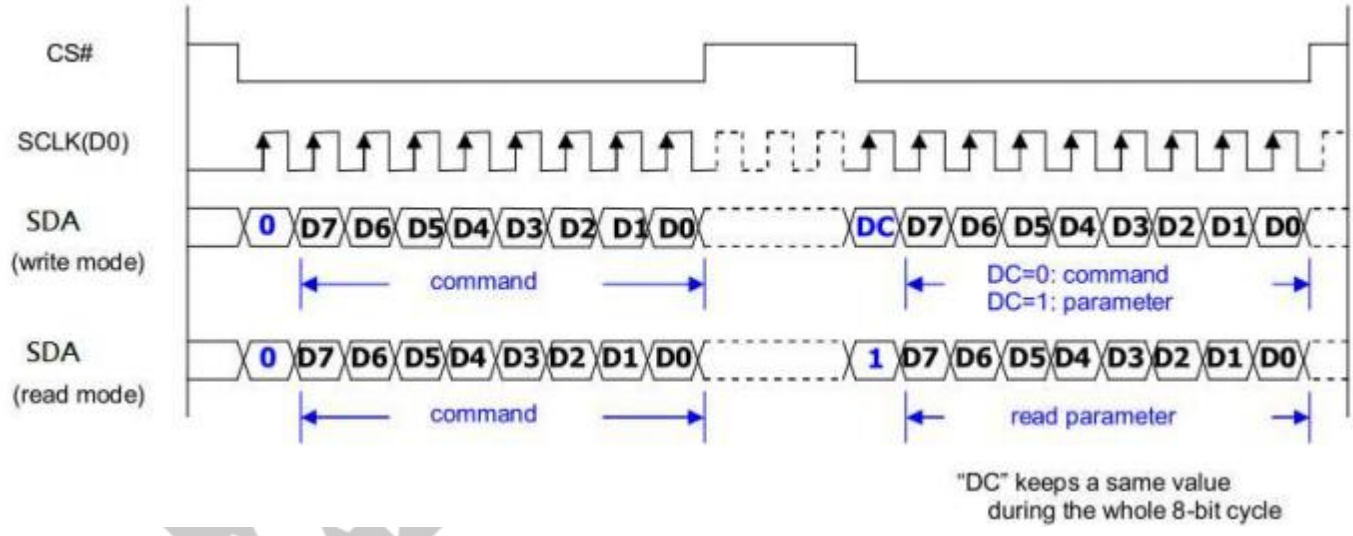


Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode

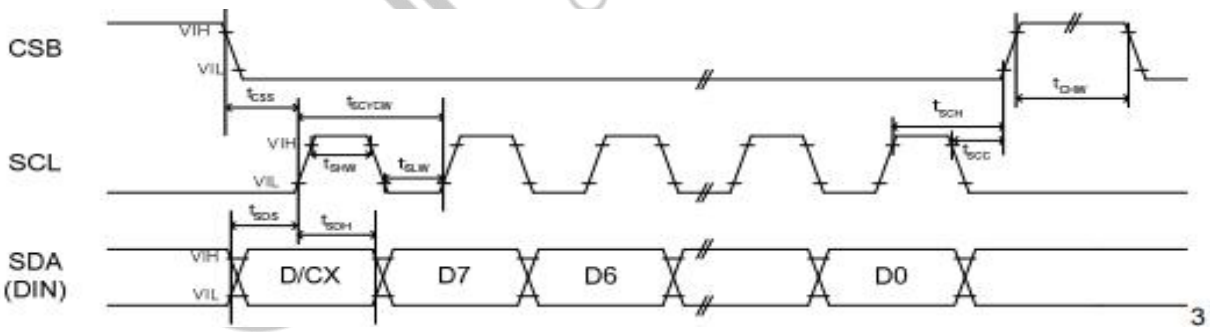
7-3-2 TIMING CHARACTERISTICS OF SERIES INTERFACE

The following specifications apply for: VDDIO - GND = 2.4V to 3.6V, TOPR = 25° C, CL=20pF
Serial Peripheral Interface Timing Characteristics

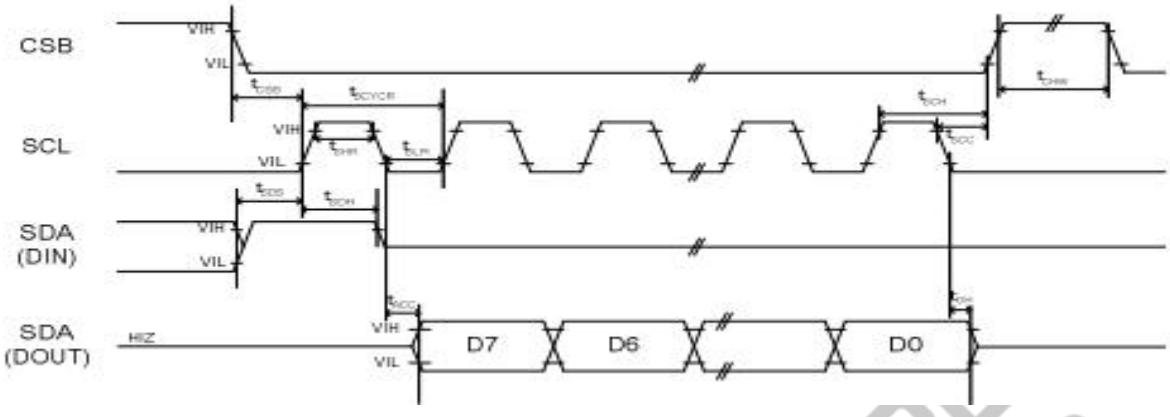
Symbol	Parameter	Min	Typ	Max	Unit
tCSS	CSB select setup time	60			ns
tCSH	CSB select hold time	65			ns
tSCC	CSB deselect setup time	20			ns
tCHW	CSB deselect hold time	40			ns
tSCYCW	Serial clock cycle (Write)	50			ns
tSHW	SCL “H” pulse width (Write)	25			ns
tSLW	SCL “L” pulse width (Write)	25			ns
tSCYCL	Serial clock cycle (Read)	150			ns
tSHR	SCL “H” pulse width (Read)	60			ns
tSLR	SCL “L” pulse width (Read)	60			ns
tSDS	Data setup time	30			ns
tSDH	Data hold time	30			ns
tACC	Access time			75	ns
tOH	Output disable time	10			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

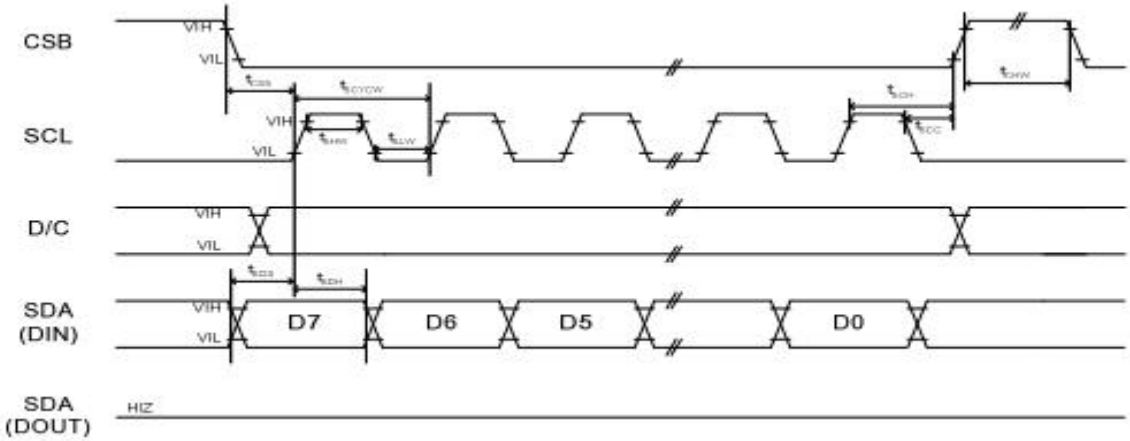
3 pin serial interface characteristics (write mode)



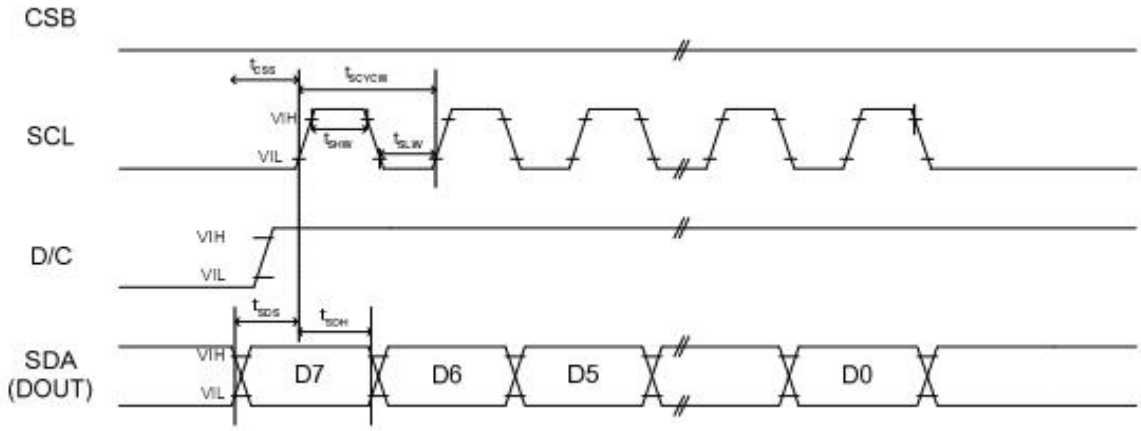
3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics (write mode)

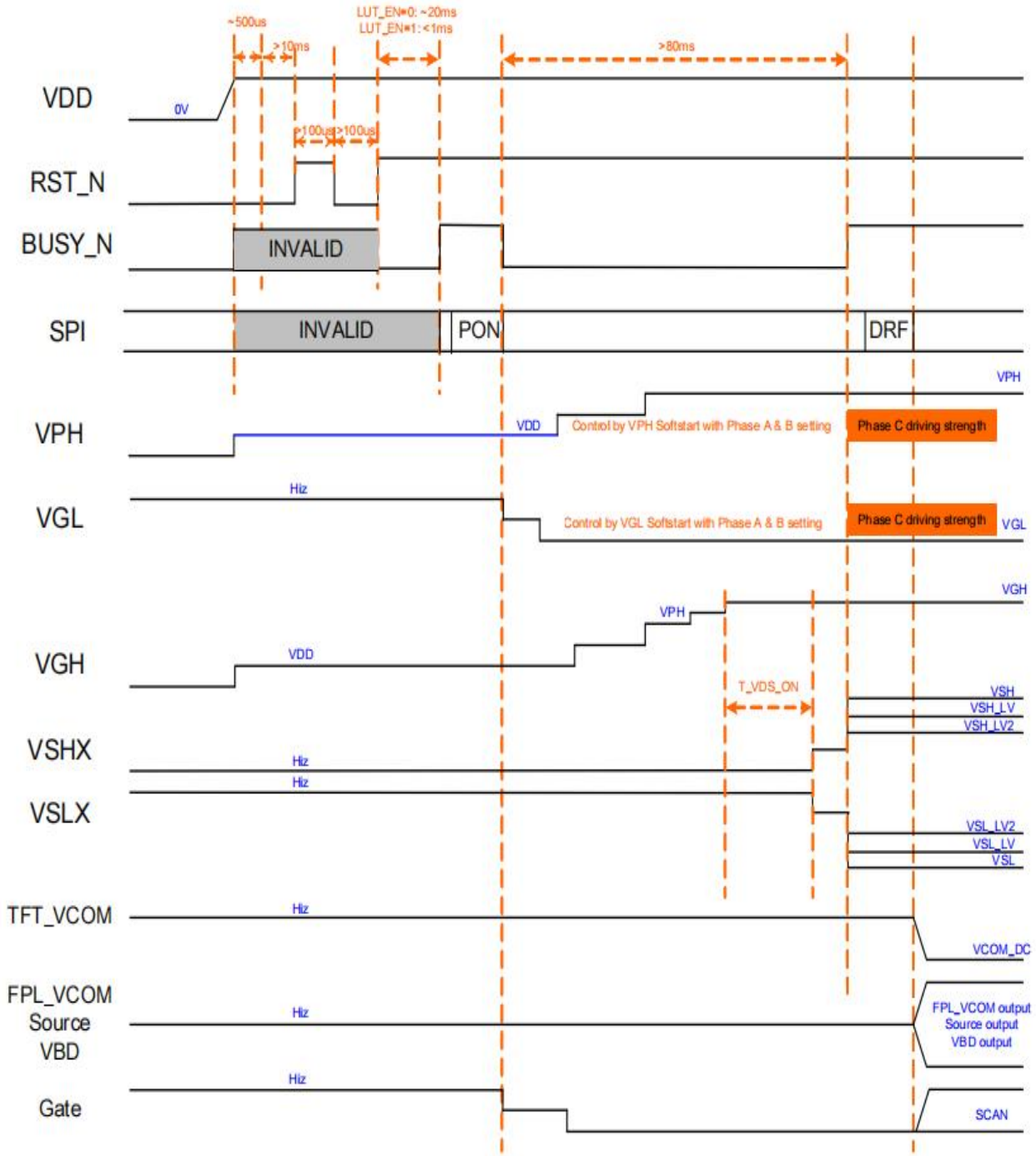


4 pin serial interface characteristics (read mode)

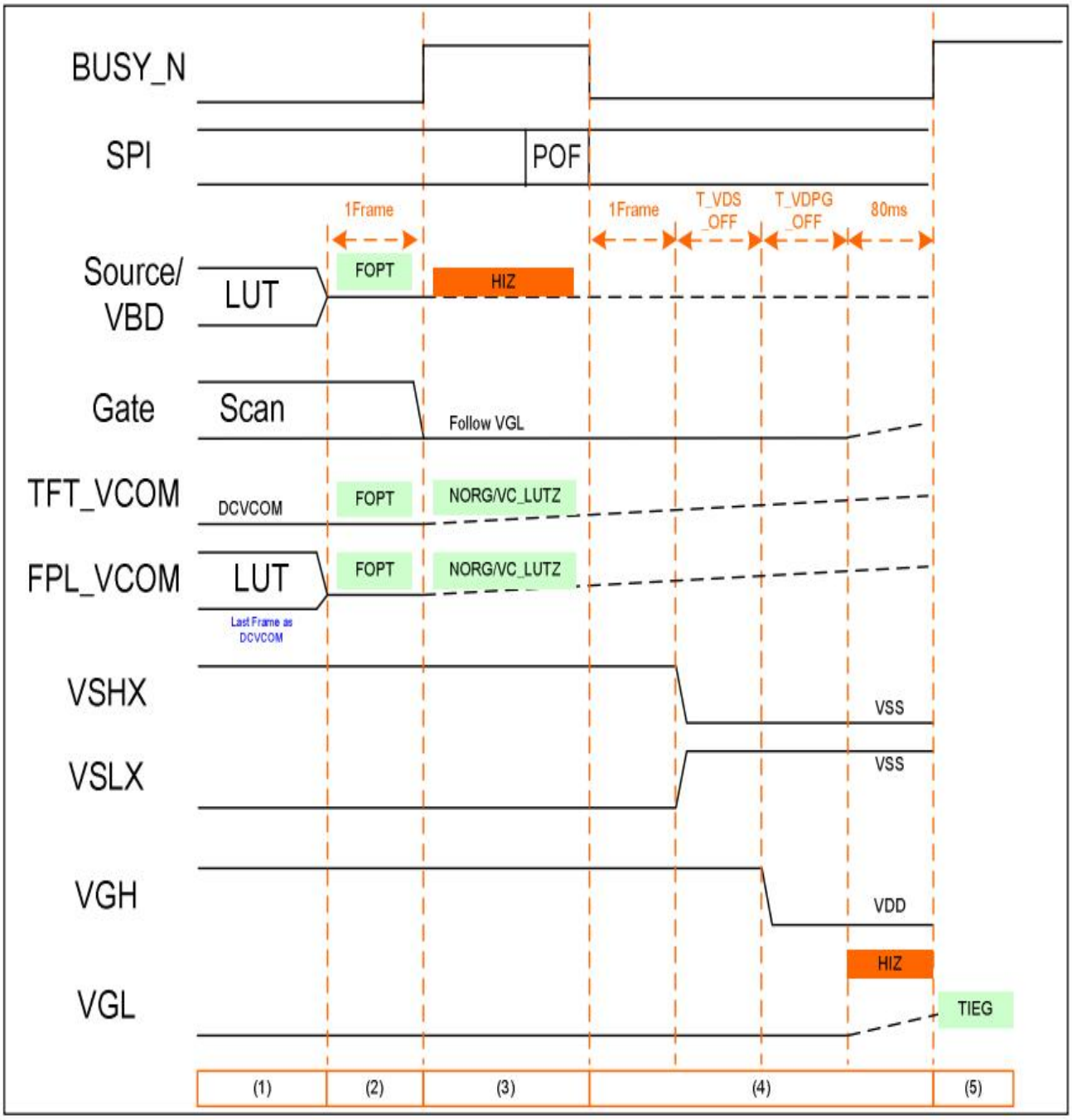


7-3-3 POWER ON/OFF CHARACTERISTICS

Power ON Sequence



Power OFF Sequence



8. OPTICAL CHARACTERISTICS

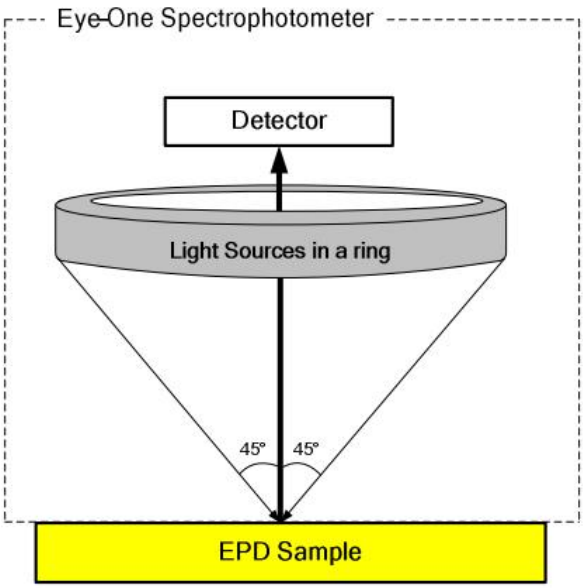
8.1 SPECIFICATION

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

TBD

8.2 DEFINITION OF CONTRAST RATIO

The contrast ratio (CR) is the ratio between the reflectance in a full white area (RI) and the reflectance in x CR = RI/Rd



8.3 REFLECTION RATIO

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{whiteboard} \times (L_{center} / L_{whiteboard})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{whiteboard}$ is the luminance of a standard whiteboard. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. HANDLING, SAFETY, AND ENVIRONMENT REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their longtime contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains tentative product specifications subjected to changes without notice.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

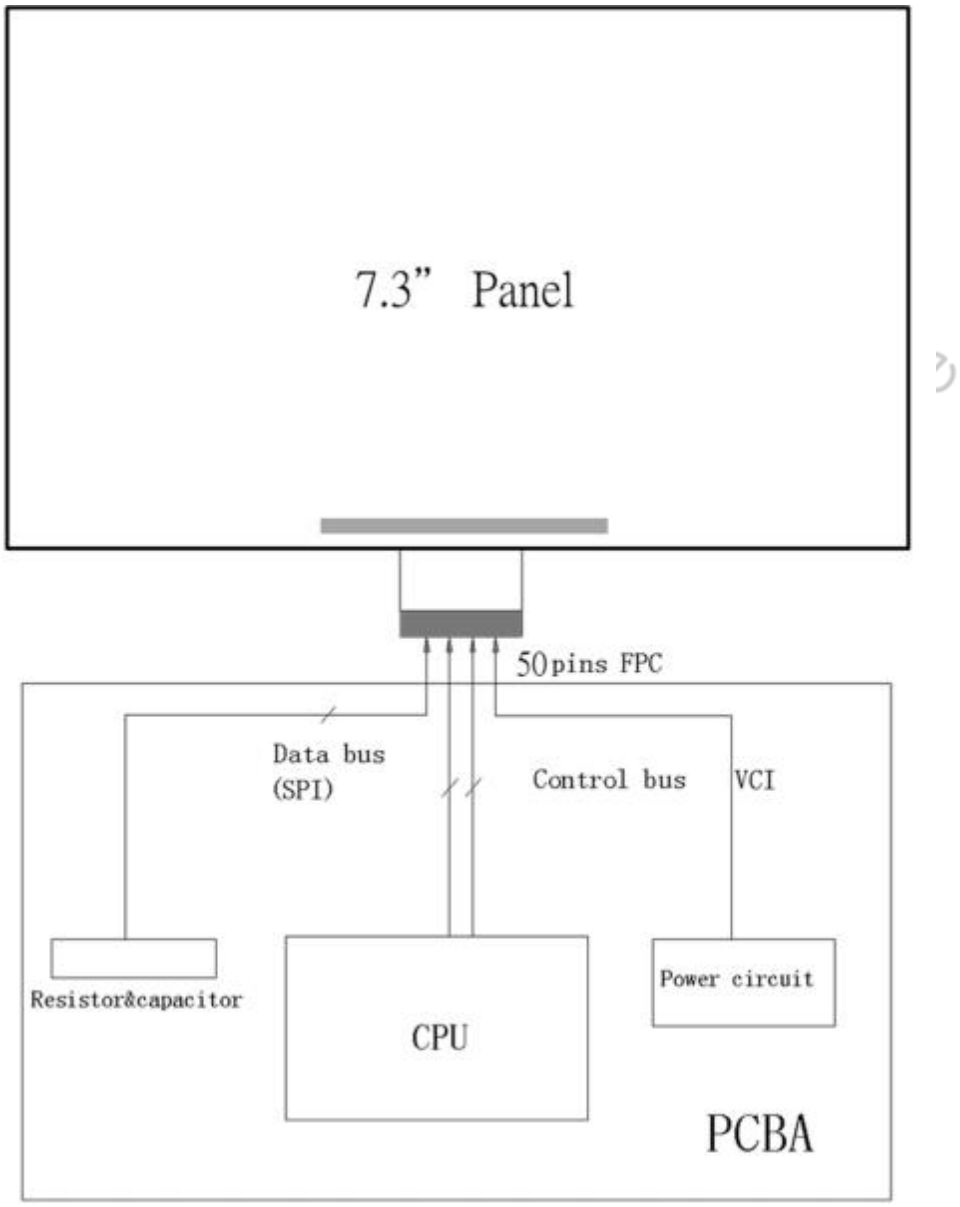
10. RELIABILITY TEST

TBD

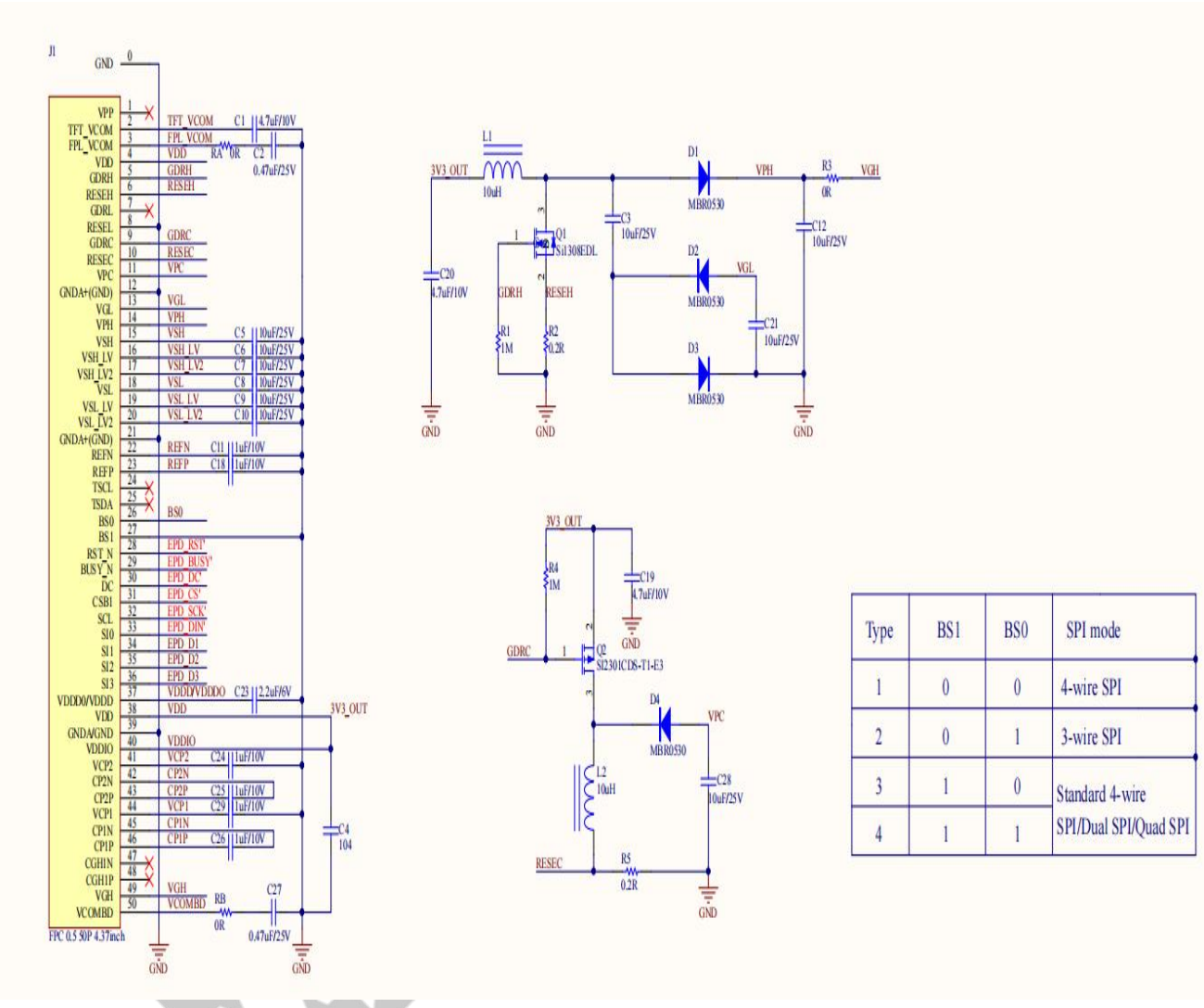
< Criteria >

In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

11. BLOCK DIAGRAM



12. SCHEMATIC DIAGRAM



Type	BS1	BS0	SPI mode
1	0	0	4-wire SPI
2	0	1	3-wire SPI
3	1	0	Standard 4-wire SPI/Dual SPI/Quad SPI
4	1	1	

13. PACKAGING

TBD

14. DEFINITION OF LABELS

TBD